

Roll No.

24165

**B. Tech. (5th Semester) (Electronics &
Communication Engg.)**

Examination – December, 2011

COMPUTER ARCHITECTURE & ORGANISATION

Paper : CSE - 210 - F

Time : Three hours]

[Maximum Marks : 100

Before answering the question, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt any *five* questions in all. Question No. 1 is *compulsory* and attempt at least *one* question from each Section.

1. (a) Describe De'Morgan's law. $8 \times 2.5 = 20$
- (b) Differentiate between SISD, MIMD architecture.
- (c) Differentiate between logical shift and arithmetic shift operation.
- (d) Compare primary and secondary types.

- (e) Define the terms : - Seek time, Rotational Delay, Access time.
- (f) Define the terms : - locality of reference, cache hit, cache miss, hit ratio.
- (g) Explain advantages of using pipelining.
- (h) Explain zero-address instruction format.

SECTION – A

- 2. (a) Design and explain the following : 14
 - (i) Half adder
 - (ii) S-R flip flop
- (b) Explain MIPS and MFLOPS 6
- 3. (a) Draw all logic gates from NAND gate. 7
- (b) Write note on performance metrics. 7
- (c) Explain the Flynn's classification of computer system architecture. 6

SECTION – B

- 4. (a) Explain any 5 arithmetic and 5 shift instructions. 10

(b) Compare RISC architecture with CISC architecture. 10

5. Explain various Addressing modes by giving suitable example for each mode. 20

SECTION – C

6. (a) A digital computer has a memory unit of $64K \times 16$ and a cache memory of 1K words. The cache uses direct mapping with a block size of four words. 12

(i) How many blocks can be cache accommodate ?.

(ii) How many bits are there in the tag, index, block and words field of the address format ?

(iii) How many bits are there in each word of cache and how they are divided into functions ?

(b) Explain Memory Hierarchy. 8

7. (a) What is the advantage of set-associative mapping over direct mapping ? State the difference between a cache line and a cache block ? 10

- (b) What are the different types of semiconductor memories ? Give their merits and demerits. 10

SECTION – D

8. (a) A non-pipeline system takes 50 ns to process a task. The same task can be processed in a 6 segment pipeline with a clock cycle of 10ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speed that can be achieved ? 12
- (b) Compare instruction level parallelism with processor level parallelism. 8
9. Write notes on : 20
- (a) Accumulator Logic,
 - (b) Various types of interrupts,
 - (c) Different micro-instruction formats.
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